Design.
For Beyond CMOS

Sandip Tiwari
st222@cornell.edu

The design process can not be considered effective and successful if
it needs PhD level experts,
or doesn't work robustly,
doesn't produce working products within spec's in first spin,
and is not open for new research breakthroughs that may be useful in technology applications.

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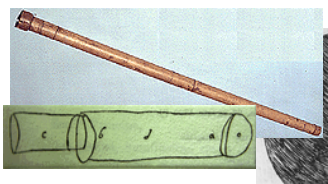
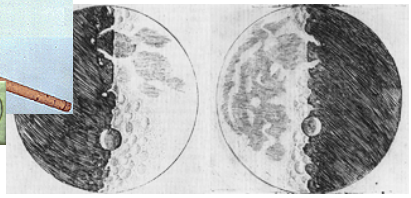
Design is Central to Good Engineering

Analog Computing circa 200 BC:
Antikythera mechanism

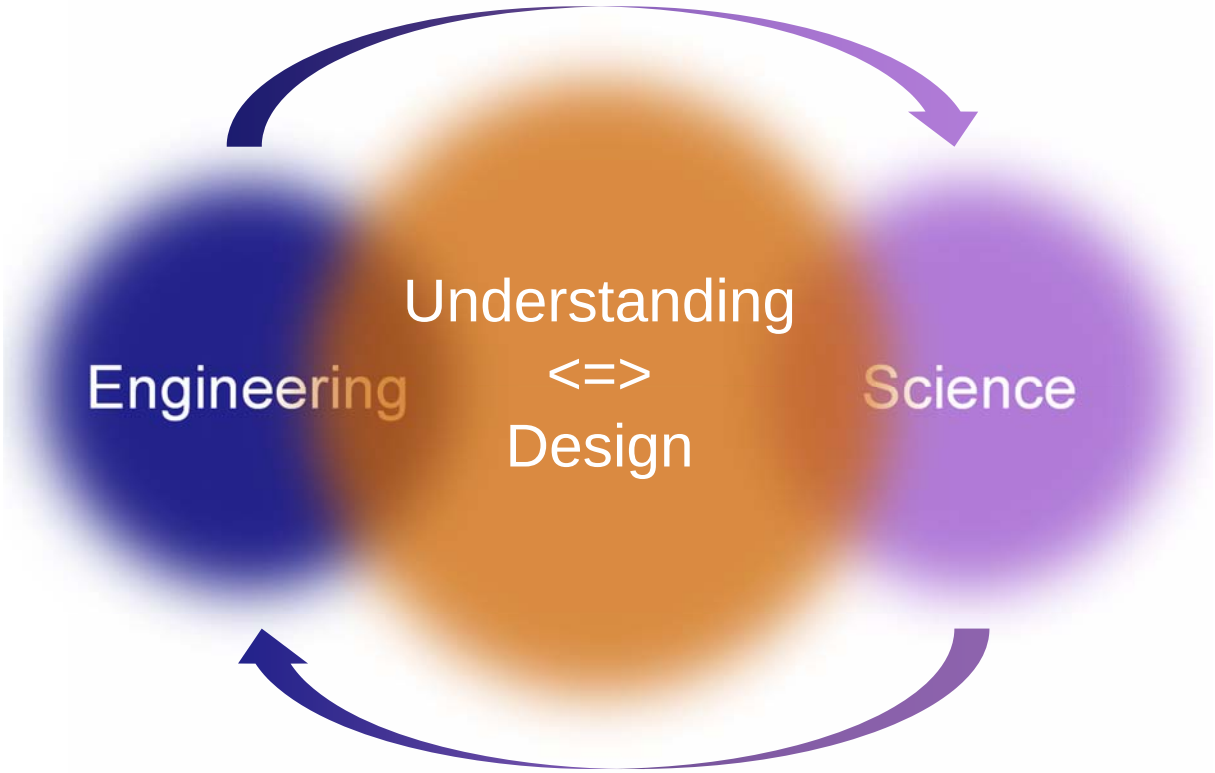
The Modern Era:
Copernicus, …

Galileo





phases of moon



Good Engineering => Good Tools => New Science => New Engineering => New Tools =>

So, what do we do today?

Digital World

High performance microprocessors:

Trillion transistors
hundreds of tools (layout, timing, process, models, noise, power, DRC, LVS, Yield, verification,)
hundreds of people
2-3 years
hundreds of milllion$'s

Embedded :

Sub-trillion transistors
hundreds of tools (layout, timing, models, noise, power, DRC, LVS, Yield, verification, …)
IP,
10's of people
1-2 years
10's of million$'s

We usually get it right first time around

Analog/Mixed-Signal/RF World

Million transistors
Even more tools
Small-signal, parasitics, tlines, large signal, cross-talk, …

With enough resources, we can design for digital with trillion transistors,

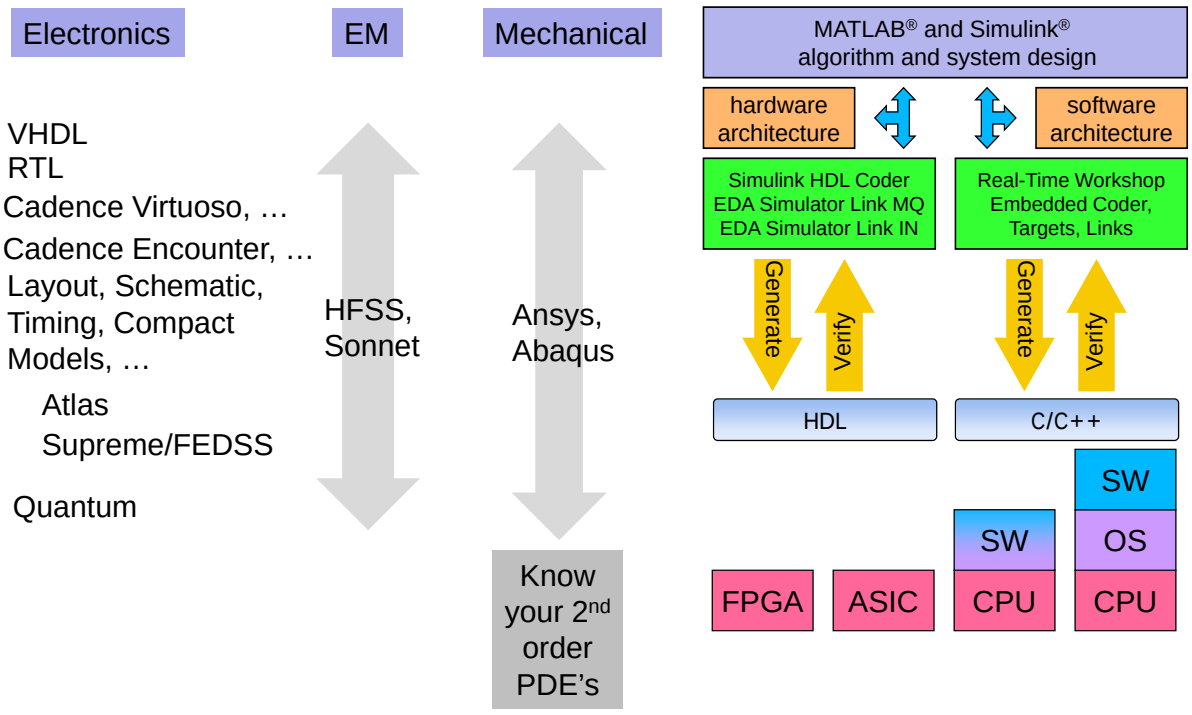
but,

can't design analog with million transistors.

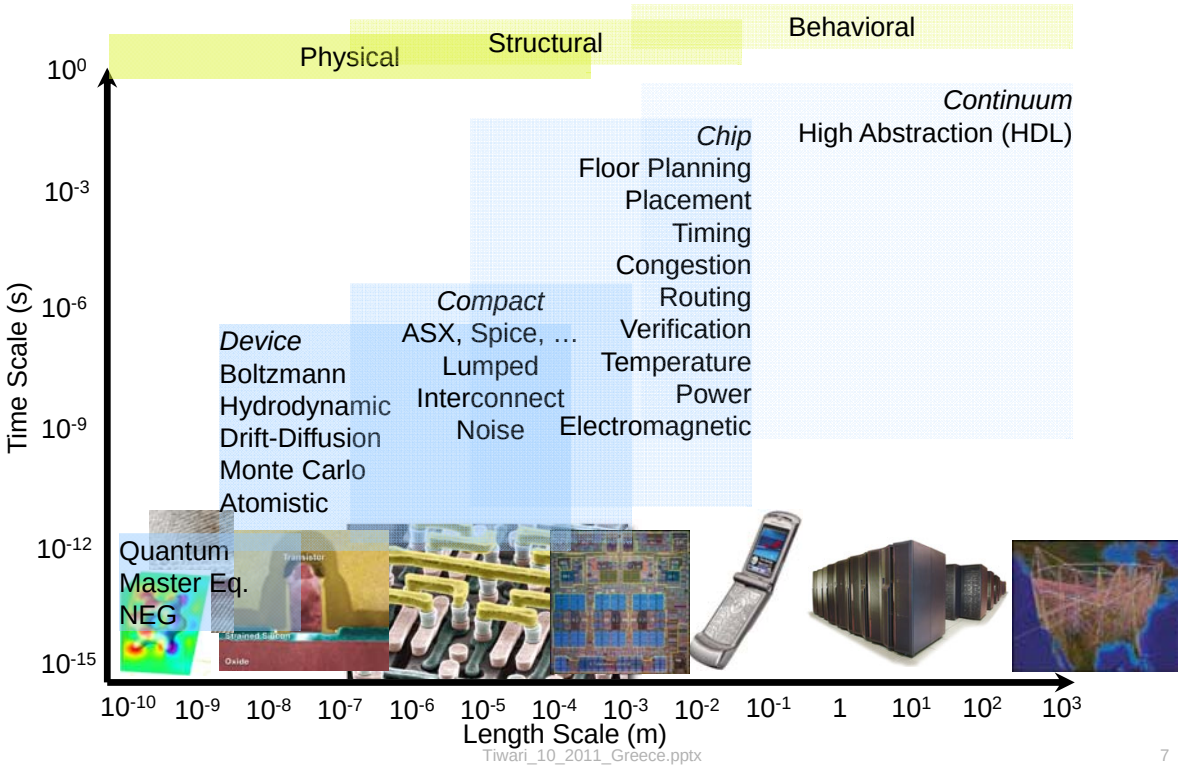
Problems with Current Microelectronics Infrastructure

- Designed for digital – is quasi-static
  - Process models – layout – 2D device – compact model for quasistatic with layout, snm, thermal, noise, statistics, ..
  - Corners for all variations
  - Designed for worst cases
  - Partitioned, Inefficient & weighted with historical baggage
- Stochasticity is intrinsic at nanoscale; it is not just a threshold variation
- Quasistatic approaches brake for high frequency
  - In-plane effects– lateral diffusions, capacitances, … parasitics
  - Digital corners and analog corners are two very different beasts
  - Small-signal, Large-signal, effects. …
- Every change, e.g., 3D, is a kluged tool to be repeatedly used with base.

Different Design Models



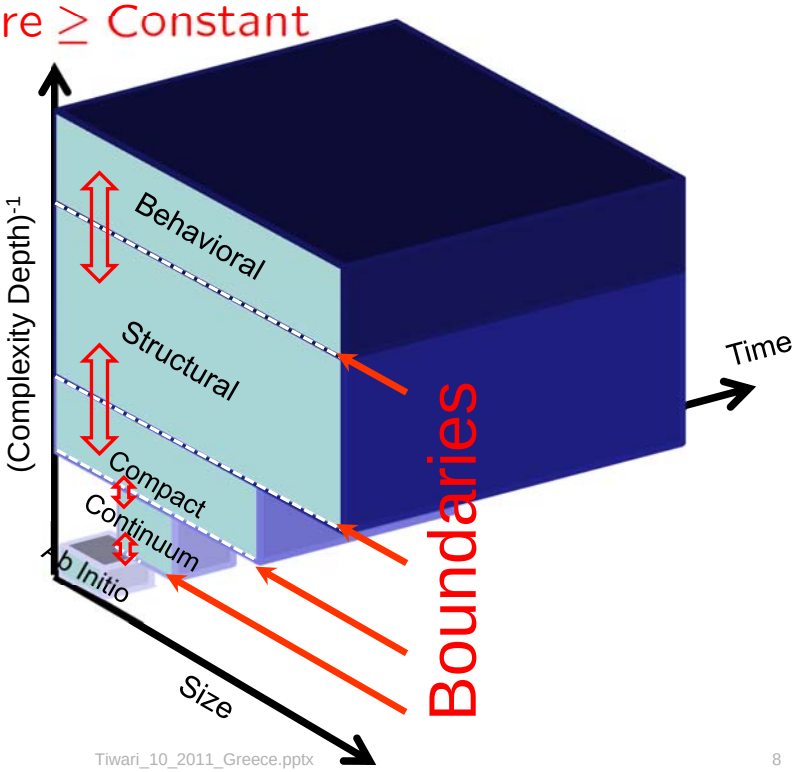
Today's Microelectronics



Design's Uncertainty Principle

$$\Delta\text{Effort} \times \Delta\text{Failure} \geq \text{Constant}$$

Let us see how we can reduce the constant of this Uncertainty Relationship



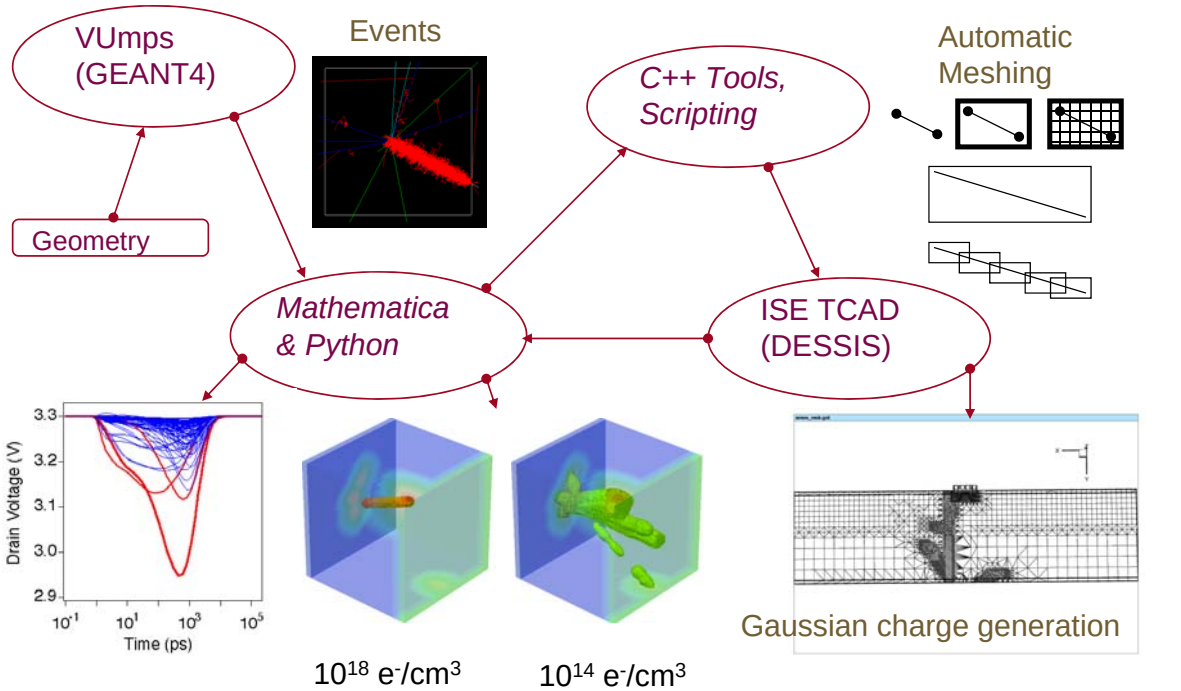
The problems of beyond?

- Signals are not just I, Q and V in *t*.
- New signal modalities and their transformations. E, H, Phonons, Fluid, Entanglement, …
- Corners at nanoscale? Stochasticity intrinsic.
- Heterogeneous integration.
- 2D – 3D
- Abstractions across scales.

Consequences

- We don't really know how to judge beforehand what works and what doesn't work?
- What is robust and what is not?
- What energy and power in changing signals?
- What are process technology interactions and effects?
- Thermal, Temporal, Length, …

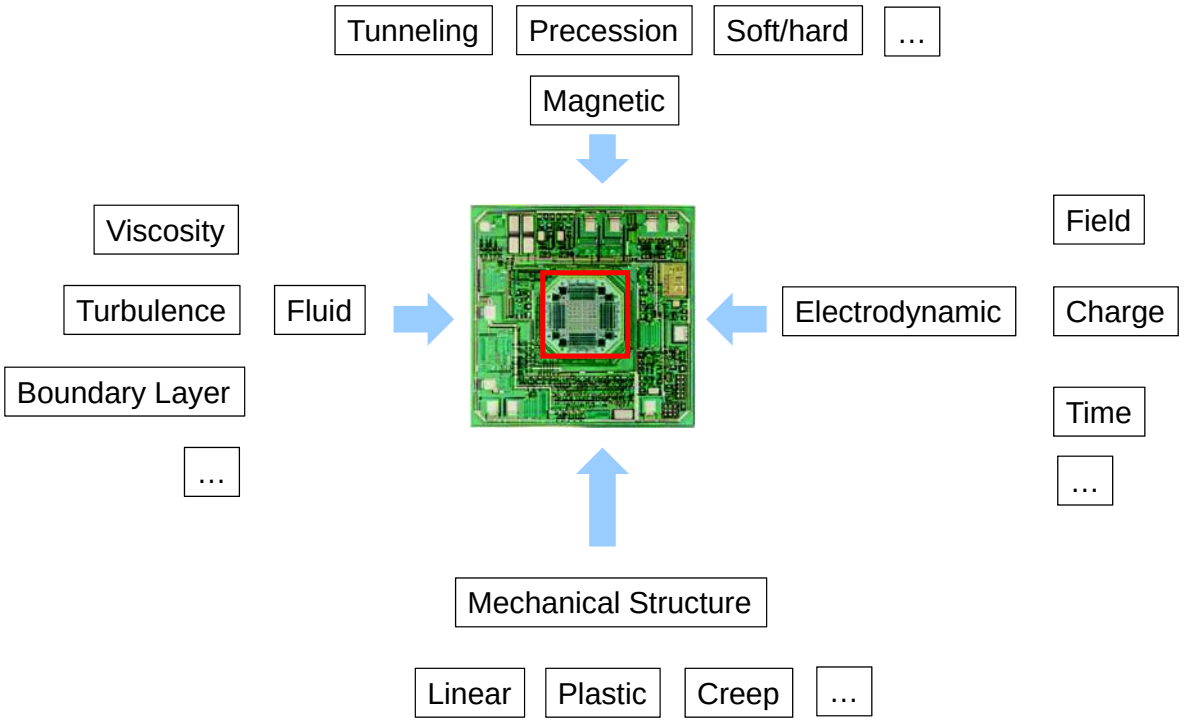
Radiation: Multiscale and Multiphysics



10^{18} e-/cm^3 10^{14} e-/cm^3

RADSAFE, R. Weller et al. (Vanderbilt)

Beyond CMOS: Fluid-Magnetic-Electric-Mechanical

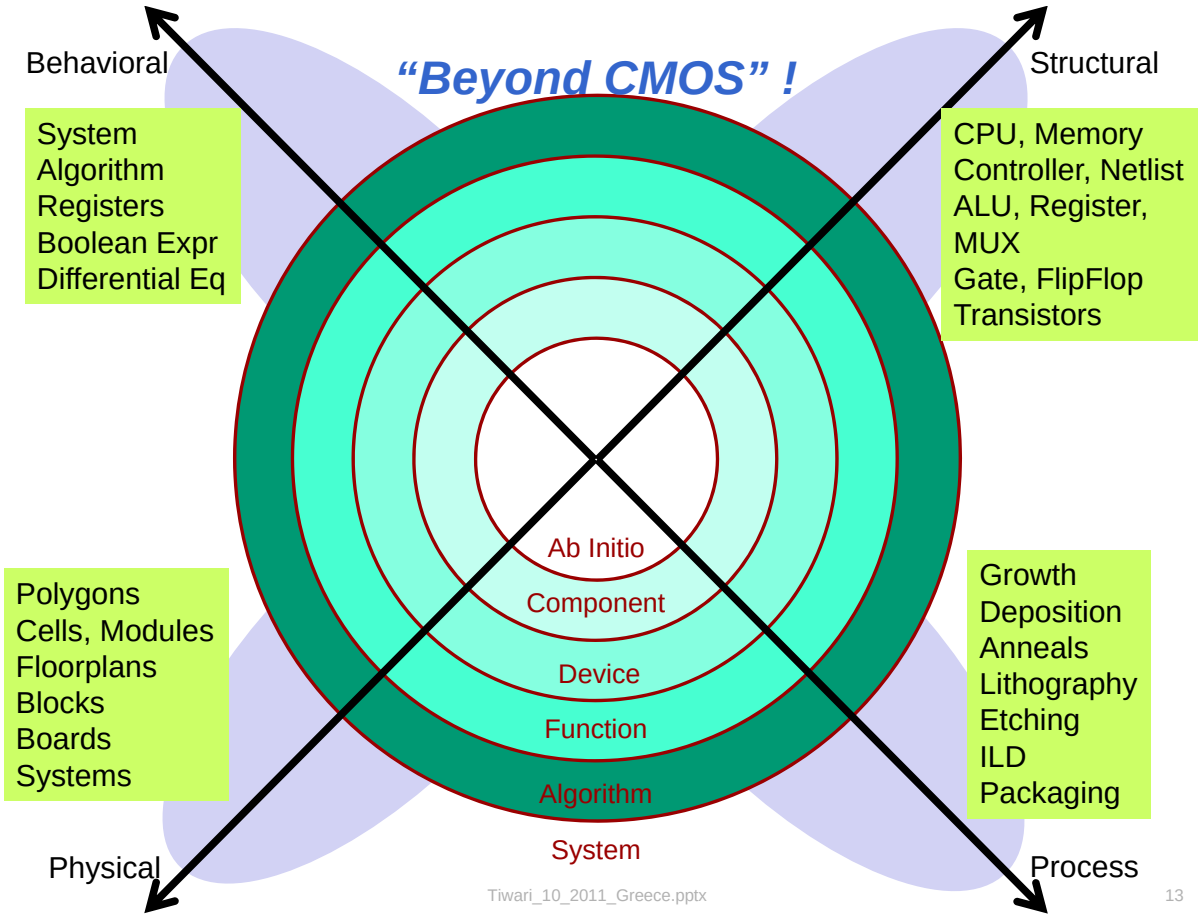


The objective of design *is* that non-specialists, with sufficient training, e.g., BS/MS, can design without knowing details of technology and everything else, so that designs can function in <u>first pass</u> with reliability and robustness.

This allows many designers (x100 or more) to take advantage of the costly technology infrastructure towards societal benefit. The technology costs are thus amortized.

The design approaches should also balance efficiencies and effectiveness.

And be open to new science breakthroughs.



New Technology Challenges

Molecular Electronics

- 100 C effects - reliability, >100 nA/μm currents, …

Solid-State Quantum Computing

- Define the system. CMOS: 1 error in 10 years in 1 switch: e ~ 10^{-20}, 10 μs

Spintronics

- μA write, Integration at length scale, spin-to-electrical conversion, …

Nanowires

- V_T control, Multi-V_T and sigma, heat, tunneling is depth sensitive – dopant tails, …

~~*Memristors*~~ *– Variable Resistors*

- Synaptic architectures not understood; refresh-decay, isn't this "hysteresis", …

Graphene

- Contact resistances 1 order of magnitude better than silicon needed. For digital, suppressing leakage, variability, surface effects, …

When the answer is negative in a fundamental form at the lowest strata, the conclusion is easy. **When it passes that test, it is much harder.**

Challenge is Global Optimization versus Local optimization under system constraints.

Late 70's: IBM stayed with bipolar because CMOS was too slow. The answer under power constraints was in architecture (similar to the multicore today). *So, system-scale design very critical.*

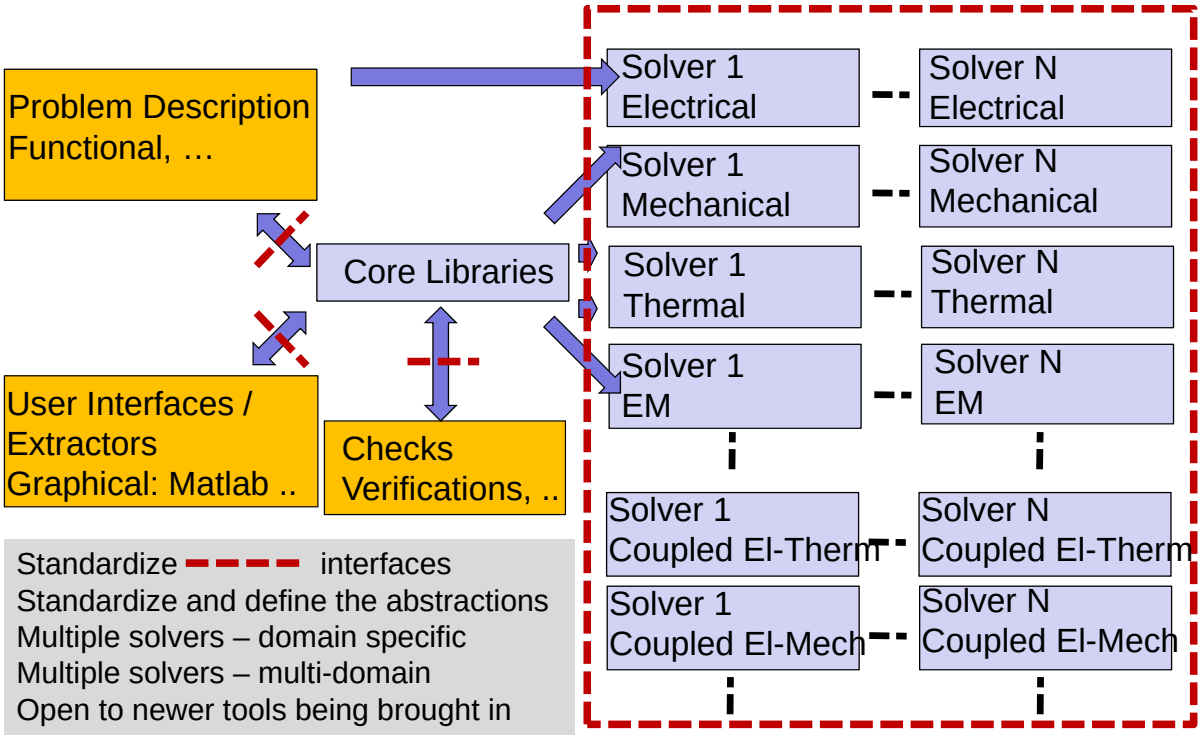
New Technology Challenges

When the answer to improvement in a subset of properties is negative in a fundamental form at the lowest strata, the conclusion is easy.
When it passes that test, it is much harder.

> *The Challenge is that if the system use is of many components interacting together*
> *Global Optimization versus Local Optimization under system constraints is a hard problem that requires a thorough design incorporating the abstractions.*

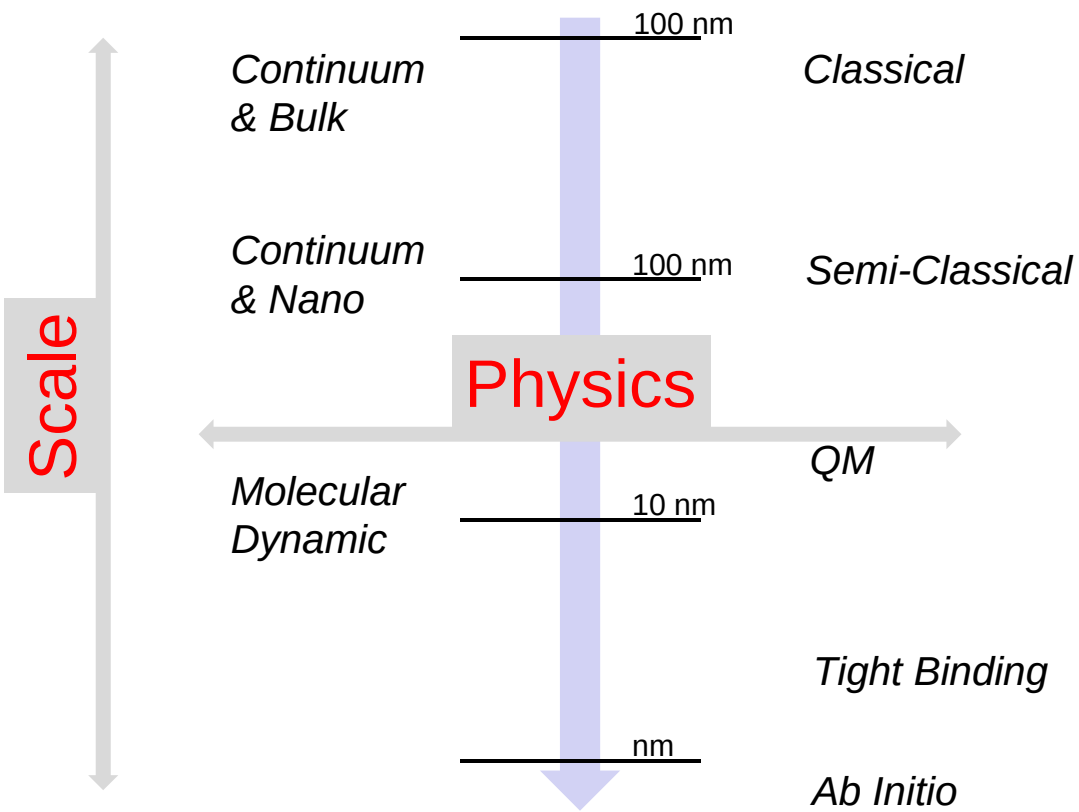
Example: In late 70's, IBM stayed with bipolar because CMOS was too slow. The answer under power constraints was in architecture (similar to the multicore today).
So, system-scale design very critical.

Build A New Open Infrastructure



Standardize ▬ ▬ ▬ interfaces
Standardize and define the abstractions
Multiple solvers – domain specific
Multiple solvers – multi-domain
Open to newer tools being brought in

Back Up


Scale
Physics
100 nm
Continuum & Bulk
Classical
Continuum & Nano
100 nm
Semi-Classical
QM
Molecular Dynamic
10 nm
Tight Binding
nm
Ab Initio