Keynote at IEEE NMDC, Oct., 2006

Energy Constrained Limits to Operation and Assembly of Information Processing Systems: Lessons for Directions of Nanoscale Systems

Invited Paper

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Abstract— Amongst the most popular questions related to information systems of today are the ones related to the search of materials, devices, circuits and architectural approaches that allow us to access and utilize the nanoscale. The broad reach of these questions leads to excessively speculative and exaggerated claims because of the nature of information processing as a complex system problem. The goal of this paper is to bring out one key theme: the centrality of energy dissipation as the primary constraint independent of property of state variable utilized for digitization of the information. When using charge transport and change of electromagnetic fields in devices and systems, non-linearity, collective effects, and a hierarchy of design across length and time scales is central to efficient information processing through manipulation and transmission of bits. We show that in the limits of nanometer scale, the dominant practical constraints arise from **power dissipation** in ever smaller volumes and of efficient signal interconnectivity commensurate with the large density of devices. These limitations are tied to the physical basis in charge transport and changes of fields, and apply equally to all materials - hard, soft or molecular - and are encapsulated in a very simple equation:

$$\tau = \frac{\alpha U}{Q A_{eff}},$$

where τ is the time constant of any energy consuming operation, U the energy consumption per operation, α the activity factor, and A_{eff} the cross-sectional area of heat removal through which heat is removed at the rate of Q. This equation points to the profound implications of size reduction. At the largest scale, the limitations arise from partitioning and hierarchical apportionment for system performance, ease of design and manufacturing. We take a hierarchical view of the underlying fundamental and practical challenges of the conventional and unconventional approaches using the analytic framework appropriate to the length scale to distinguish between fact and fantasy, and to point to practical emerging directions with a system-scale perspective. **I argue that Adaptive Electronics focusing on power dissipation at nanoscale is the need of the hour.** Examples of possible approaches are shown.

Keywords - Energy, Adaptive Electronics, Defects, Nanoscale, Performance.

I. INTRODUCTION

Limits of electronics, because of its immense importance, has been the subject of many detailed and excellent discussions[1-5]. In this work, we approach the issue of nanoscale from a perspective of complexity in order to outline the frame-work and the key issues that arise from use of electron transport and electromagnetic signal transmission across wires in an assembly of a large number of components. This complexity of electronics arises from coupling of disparate scales: (a) from devices at nanometers to supercomputers of 10's of meters, (b) time scales ranging from femtoseconds for individual electron events to milliseconds for non-volatile memories, programmable chips, and internet interconnectivity; and (c) coupling of domains with interconnections between algorithms and data management derived from computer science with implementations that are derived from physical sciences and engineering. Tera-scale densities link the non-linearity and sensitivity of large interacting components with that of the network in determining the system behavior. We will outline here some principles that emphasize the inherent complexity of this problem and the principal barriers to the one expectation we all have of an information processing system – total predictability and reproducibility. We discuss the physical behavior first and then relate it to robust design, to draw our conclusions.

II. COMPLEXITY: LENGTH, TIME AND ENERGY SCALES

Energy loss in charge transport and changes in electromagnetic fields are intrinsic to the device-level information processing and the information flow in circuits and systems. The poor scaling of voltages and the importance of current in driving wires is well recognized. As sizes scale, the importance of this dissipation in ever smaller volumes and areas increases. The time constant of any energy consuming operation (τ) can be related to the energy per operation (U), the activity factor (α) and the cross-sectional area of heat removal (A_{eff}) through

$$\tau = \frac{\alpha U}{Q A_{eff}},$$

where Q is the heat removal rate. This is a very general relationship independent of the specifics of device or circuit. Heat removal rate of 100 W/cm^2 average and 10^5 W/cm^2 localized peak is possible in silicon due to its good thermal conductivity (148 W/m.K in bulk Si). The challenge at nanoscale arises from the non-scaling of energy dissipation with area. Current transistors (~100 nm scale) dissipate ~ 2×10^{-16} J, or ~50,000kT per operation while a 10 nm length scale device is likely to dissipate ~4×10^{-18} J or ~1000kT per operation based on their expected current drive capability, sizing and noise-margin-compatible voltage span. This is a change of ~50x for an area change of ~100x. This implies that either the activity factor needs to be slowed down or the effective area increased, else, the temperature rises. Temperature is an issue in today's designs and maximum local temperatures in high performance chips cannot be allowed to rise any further. The current designs handle the temperature issue in the fastest devices – clocks, registers, ALU elements – by a spreading flow of heat (higher Q) and by an increased effective area due to the large number of intra-circuit interconnections. This leads to time-constants of a few ps, such as in high performance logic devices, to a few 100 ps, such as in arrays of SRAM, DRAM etc. for the individual cell delays. The implications for new technologies - carbon nanotubes, organic and molecular structures, and even silicon-on-insulator (SOI) where Q decreases from poor conductivity of SiO_2, is that the design space of operation has to be consistent with the energy dissipation – time constant – heat extraction relationship. SOI has reduced Q and U, carbon nanotubes may have specific consequences from lower A_{eff}, while organic materials may need to operate under conditions that are consistent with lower sustainable temperatures than of silicon. The hierarchical organization of the integrated circuit and the parallelization of information processing are critical to the high speeds that information processing achieves within this power and time-constant constraint.

Digital electronics requires information to be detected and restored; this too places energy constraints on operation. In memories, voltage sensing employs a pre-charged line flipping by ~100 mV[1] while current sensing needs 10 to 40 μA of current for detection in a few ns. DRAMs, with ~40 fC of charge being detected on the capacitor, have a non-scaling energy of ~4×10^{-15} J ($10^6 kT$), and SRAMs, with current-sensing, have a non-scaling energy of ~10^{-14} J ($2 \times 10^6 kT$) per bit read. What makes the memories low power is the infrequent (low α) access of the bits.

[1] This "memory sensing noise margin" is consistent with a voltage tracking of ~20 mV and a sensing time-constant of few ns. In digital logic, each gate is itself a sensor and amplifier, and thus needs to be significantly faster and much more compact. These time and length scales constrain the noise margin to exceed ~200 mV.

Irreversible energy dissipation is necessary to achieving direction to transition between the states and to maintain the distinctive states. Equally important to achieving direction to transition, and hence isolation of input, is the use of more than two terminals in any active device[6].

Energy also enters the discussion of nanoelectronics through the robustness and electrical characteristics of structures, and the amenability to structured hierarchical design that supports useful performance. Semiconductor processing used to build or modify materials and form their interfaces employs activation energies on the order of eV and above[7-9], and for processes critical to interfaces and surfaces such as diffusion of dopants of many eV[10]. So, by necessity, fabrication employs high temperatures, usually 700 C or more, which in turn provides robustness at device operation temperatures. Organic and molecular self-assembly processes occur at 0.1 - 0.5 eV energy scales[11,12]. This lower energy is not intrinsic to self-assembly, oxidation of silicon is a self-assembly process with ~2.26 eV activation energy, but because the organic molecular processes employed to assemble structures have to be compatible with stability of the organic materials. Stochastic variations that result from these fabrication processes have an exponential relationship to the probabilities ($\exp(-E_a / kT)$ dependence on the activation energy E_a). Lower activation energies imply wider spread which in turn necessitate error correction and fault tolerance in implementation. Self-assemblies also exhibit short and long range order commensurate with these activation energies. This order also exists in semiconductor epitaxial growth[13], another example of a self-assembly process usually performed at high temperatures, but which has little consequence on device behavior because of secondary effects on band energies and transport at large domain sizes. In molecular structures this does not necessarily have to be so because of the lower activation energies, and hence broader probability distribution functions result. The probabilistic connection through variations in device characteristics is exemplified in a static CMOS inverter by a failure probability of $\exp(-2V_{DD} / \sigma(V_T))$, where V_{DD} is the bias voltage and $\sigma(V_T)$ the variance of threshold voltage[14]. The limitations on n-channel only, p-channel only, pass transistor, various early diode-based logic, Josephson junction logic, and the variety of logic schemes attempted in III-V semiconductor technologies all arise from the limits on length-scale of integration placed by these failure probabilities, the effect on time-scales of device variations, and in the case of diode based approaches the additional failure in maintaining sufficient directionality to information processing flow.

The field-effect transistor typically has an energy barrier of ~eV in off-state (between source and drain), which is lowered for conduction in the on-state. During conduction, transport occurs with barriers absent in the flow path while the carriers are confined by regions of large barriers (SiO_2/Si interface, or insulator/nanotube e.g.) laterally. The carriers themselves flow uninterrupted by a barrier in between the conducting contacts. Conduction in molecular organic structures either relies on energertics that is strongly mediated by the molecular bonds –

examples of these include conduction that is highly non-linear with bias, or by hopping transport. One implication of this is that active currents are low even when current densities are high (a nA of current in a single molecule is a current density of ~10^6 A/cm^2).

Another overarching factor in discussion of electronics is that of interconnections or wiring. We will discuss this in the context of massive integration later, but a primary question in device-signal transmission interaction is that of impedance. Free-space impedance of $\sqrt{\mu_0/\varepsilon_0}$ is ~377 Ω, and the present practice of interconnects leads to impedances that are about factor of 10 lower due to geometric considerations. Resistances of wires are kept small to minimize RC delays as well as voltage drops in order to minimize error probabilities. Nanowires need to be highly conductive for any approach using electronic transport to be successful. Scaling of metallic interconnects in order to improve bandwidth and latency through organization of architectures and implementation of technologies has been a constant focus of electronics technology efforts. Nanotubes, currently viewed as one possible means to achieving highly conductive wires, can potentially achieve $h/4q^2$~6.5 kΩ of resistance in ballistic limit. If one considers only the fringing capacitance (~1 pF/cm) for these wires, this implies a delay in the limit of approximately 6.5 ps/10 µm of signal propagation distance, and the impedance is too high. Bundles of nanotubes are necessary in order to reduce the resistance. Wires made from metallic materials should be expected to be significantly less conductive due to scattering and will result in significantly larger delays and voltage drops.

This short discussion emphasizes the following:

a. Currents of the order of 10 µA and higher are needed for sensing memories at ns time scales.
b. Energy changes of at least ~1000kT are necessary to achieve irreversible reproducible binary computation.
c. Power dissipation in decreasing area with size requires an adequate architecture that can bring about the necessary performance without compromising temperature limitations.
d. Energy scales are important to achieving adequate control of the device formation and device operation.
e. Interconnects and wires require reasonably low impedance and resistances for them to be useful even with adequate hierarchy in design.

Our discussion will now build on the intersection of constraints from the low dimensional limit of single device with the high dimension limit of highly dense system.

The $\sqrt{n}$ Problem: Effect of Large Stochastic Variations

In a stochastic distribution of n particles (atoms, dopants, defects, electrons, interface bonds, …), the distribution is subject to fluctuations which in turn causes properties such as energies, scattering, conductance, … to vary. The ratio of standard deviation to mean of these properties varies as $1/\sqrt{n}$. An important example of this, already a major challenge for electronics today, is the variance in threshold voltage of static memory cells arising from dopant fluctuations. For a variety of properties important to the operation of the devices, Table 1 shows the relative variance. The yield of a chain of m elements with these properties has a net yield of $Y = (1 - p_f)^m$ where p_f is the probability of failure of a single element.

Table 1: The 3D, 2D and 1D relative variances resulting from decreasing collective effects at small dimensions.

	10 nm	5 nm	3 nm	1 nm
3D:*Bandgap, Threshold, Junctions, Capacitances, …*				
n	~28000	~3500	~750	28
$\sigma/\bar{n}$	0.6%	1.7%	3.7%	19%
2D:*Inversion charge, Interface defects, Contacts, …*				
n	920	230	83	9
$\sigma/\bar{n}$	3.3%	6.6%	11%	33%
1D:*Wire resistance, Wire defects, Molecular contacts, …*				
n	30	15	9	3
$\sigma/\bar{n}$	18%	26%	33%	57%

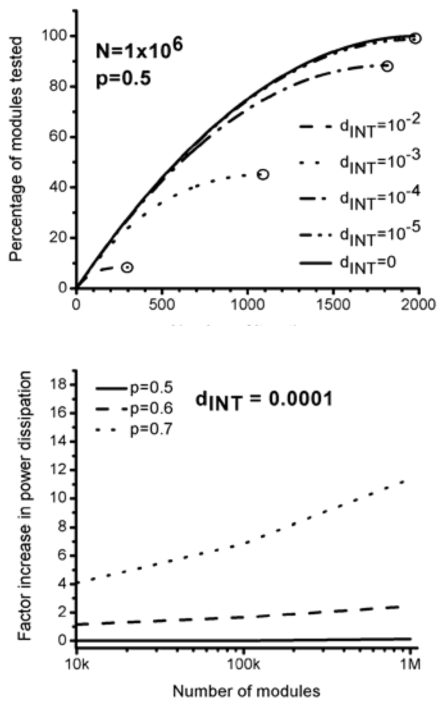
This table emphasizes the increasing variations at smaller dimensions that circuit and system design must handle in order to be robust and then extends it to the case where the dimensionality of the structure is changed. An example where these statistical variations require hierarchy in design today is the use of steering logic (pass gates e.g.) to a certain level of integration before restoring levels with static logic. Steering logic, while fast, is subject to signal degradation due to the variations. Within the integration limits placed by the yield, restoring functions allow recovery of the signal. This table emphasizes the importance of the significant scaling up in variation of properties that occurs as one goes to lower sizes and lower dimensionality. While today's transistors may be expected to have ~1% relative variation each from different causes – dopants, gate lengths, background doping, insulator thickness, work functions, etc., the problem is exacerbated by a power relationship at smaller length scale and dimensionality. Where properties are dependent on smaller dimensions – interface to molecules, conductance of one-dimensional wires, these variances are significantly larger and therefore the challenge to hierarchical design to work around the related limits significantly stronger.

Hierarchy in Design: Top-down and Bottom-up

Hierarchical design has been central to the practice of electronics in solving the problems of yield. Memory structures employ redundant arrays and redundancy is also employed in many high performance oriented dynamic circuits. Use of molecules as currently envisioned in electronics[15-18], with their small size, shape and functionality brings many of the stochastic effects but not the distinguishable reproducible states that are possible with three-terminal gain elements. Fragility, charge state's dependence on current flow, dependence of stability on charge/oxidation state and temperature, interfacing which is subject to the limitations of the Table 1, short and long range order, broadening of levels with contacts inducing gap states, broad line shapes, and the need of energy barriers to provide stable electronic state, all create difficulties in achieving appealing device characteristics for the bottom-up approaches. Another important point is related to assembling with hierarchy. Self-assembly has short and long range order and results in a single ordered array as the best possible outcome. This is useful in ordered electronics – such as memories, but troublesome in logic since externally imposed hierarchy is needed for the system to achieve robust design and useful performance.

We discuss these issues with an example of the penalty in configurability in electronics since configurability is one of the potential solutions to achieving robust designs in presence of defects. Field-programmable gate arrays (FPGAs) have widely been employed in electronic systems due their ease of configurability. Approaches have been outlined [19] to designing with defective molecular systems. The problem is complex because of the importance of interconnectivity in achieving speed and power attributes desired, but equally important and restrictive is the issue of working around defects once defects exceed a certain critical density. Key to working with defects is testability and design around defects.

Figure 1: Observability in the presence of defects: percentage of modules tested for different interconnect defect densities. (a) shows the percentage of modules tested as alt of interconnect defect rate with 1 M logic blocks and (b) the factor increase in power as a result of increasing area of devices.



For any logic block, the terminals provide access for this testing and their count is related to number of gates at all hierarchical levels through the Rent's relationship $T = tN^{p}$, where t is number of terminals per logic block and p a parameter of compressibility – how well a circuit has been optimized (p=1, e.g. is entirely non-optimized with all terminals available). A smaller p compresses the information available from the unit. Through iterative testing, one penetrates deeper into an array and identifies defects. In each iteration, only a fraction can be tested because of the compression. If t terminals are required to diagnose a logic block, then Rent's relationship tells us that $tN^{I}_{accessible} \sim T$ in iteration I, i.e., $N^{I}_{accessible} \sim N^{p}$. After iteration I, $N - N^{p}$ units have been tested, and the number accessible for testing in iteration II is $tN^{II}_{accessible} \sim T(= t(N - N^{p}))$ or $N^{II}_{accessible} \sim (N - N^{p})^{p}$. The power relationship, similar to that in yield, appears. A defect has a very non-local effect – it makes a larger group of devices and interconnects inaccessible for use since they cannot be tested. The consequence of higher defect rates is a power relationship in number of testing cycles, in area and power to achieve the necessary logic depth, and finally speed because of the increased area in order to achieve a certain number of blocks to work with. Logic defects have a smaller penalty because they affect N; however, interconnects have much larger penalty because they render a larger group unavailable for testing (through the proportionality factor t). Figure 1[21] show this penalty for a simple example - the consequences of defects in interconnects. An additional important consequence of defective terminals is that not all logic modules can be tested irrespective of whether they are functional or not.

These calculations show that there is a large penalty in usability of resources, in power dissipation, in speed, and other attributes as a result of working with defect levels even at 0.01%.

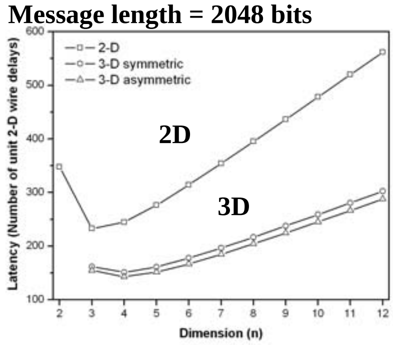
The use of hierarchy, steering logic combined with restoration logic and the partitioning of designs with specific task oriented functional units, is an approach that is natural to working with limitations placed by power, noise-margin, timing, and desired speed, that one encounters in electronics as a complex system. With the short-range and long-range order expected in molecular self-assembly process, and the variability, a hierarchical design will be required to allow design and operation while working within the limits of the technology. This is going to be a very difficult if not an insurmountable challenge.

The easier problem to address with molecular structures may be ordered arrays where the molecular elements are passive elements and where we employ them in sufficient numbers to improve on the relative variance of the characteristics. Some of the electronic memories are examples of largely ordered arrays that can employ passive elements of unique characteristics operating in nanosecond time range under a different set of power constraints. This objective of memory places a different set of constraints on the operation that may be more easily achievable.

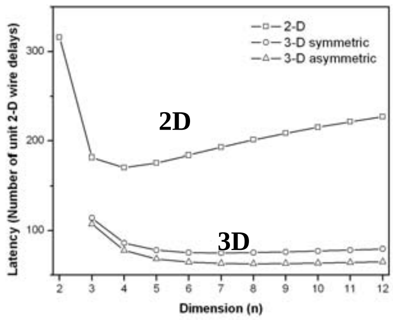
Complex systems have another characteristic that we have not considered to this point: adaptation. Nanoelectronic technology will need to adapt to the two limiting attributes we

Figure 2: Network on chip as an approach to working with extreme levels of integration – 10^{10} to 10^{12} devices. The graphs show performance from designs with 10 nm minimum length scale devices for different message lengths used in the network. The network consists of *N*=4096 nodes with radix *k* and dimension *n* ($N=k^n$).

Message length = 2048 bits



Message length = 64 bits



have discussed in some detail: power and variability. Some of the electronic approaches increasingly being accepted today: use of multiple supply voltages, sleep modes that turn off sections of a chip, design of pass logic together with static, changing of threshold voltage using back-bias, variable multiple frequencies, etc. are examples of adaptation in practice. We should anticipate that power constraints as well as increased variability would bring new approaches to designs where adaptation at device, circuit and system level will play an increasing role.

III. COMMUNICATION: INTERCONNECTION OF LARGE NUMBERS

The 10 nm physical length generation of devices is predicted to be capable of 10^{10} to 10^{12} devices. If system design techniques do not change, the communication between the devices and their interconnectivity will thoroughly dominate the behavior of the system. The emphasis of the system design therefore needs to place increasing premium on adaptively working with these large numbers. The chip increasingly appears as a network. Reduction of latency, improvement of bandwidth, and emphasis on a communication structure that provides the appropriate time-scale of information transfer are attributes that take on similar importance as that of hierarchy in the design. Systems designed akin to communication networks employing ideas of data hopping between modules, increasing logical partitions of nodes, large interconnectivity, may perhaps help with achieving robust system behavior.
Figure 2 shows two examples, employing different message lengths, and assuming a technology generation employing 10 nm minimum physical length scales. In such a system, based on projections of the ITRS roadmap, it would be possible to design with 4096 interconnected nodes, each node consisting of 3.4×10^6 transistors, with a global RC delay of 618 ps/mm and a clock cycle of 45 ps with logic depth of 16. Reduction of dimensionality of the design is critical to achieving adequate system performance by emphasizing the communication bandwidth.

IV. WORKING WITH STOCHASTIC VARIATION AND INTERCONNECTIVITY

We conclude with a few examples[21-24] of how nanoscale structures are evolving to handle the issues discussed. Working with stochastic variations, reducing power by adaptation, hierarchical design, and finding approaches to achieving higher interconnectivity and bandwidth are all examples where technical directions are increasingly becoming clear. Statistical variations have to be minimized and the length scale of integration is related to the error probabilities of the variations. Non-volatile memories, e.g. benefit from a larger number of defect nodes for storage of charge detected through the transistor's conduction.

Interconnectivity is a key problem whose present evolutionary solution appears to lie in three-dimensional integration that affords a third direction for short interconnectivity. Three-dimensional integration is also an interesting case study in hierarchical design – a form of system on a chip using the third dimension. But, the major constraint here arises from the accumulation of power dissipation in multiple layers as also of only specific architectures and applications benefiting from integration.

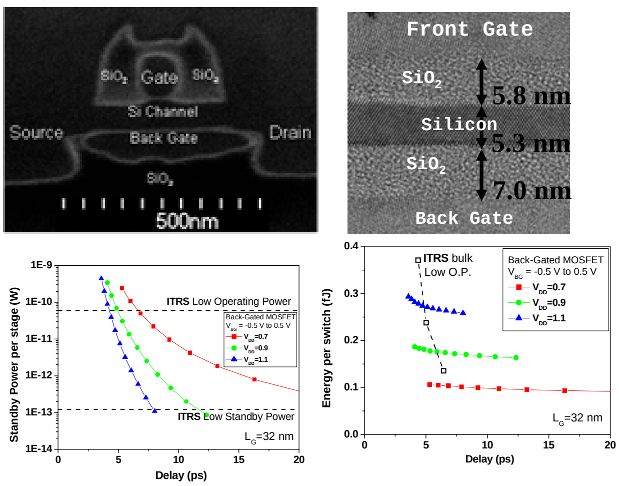
The second group (b) shows a thin silicon channel based geometry where a back-gate voltage provides tuning of transistor characteristics at similar time scales as the transistor operation and thus brings the capability of adaptation for power and speed to the device, circuit and functional unit level.

V. THE FUTURE: FOCUS ON ADAPTIVE ELECTRONICS

Hierarchy in design, controlling power, providing improved interconnectivity, and achieving smaller variance through collective effects are common threads towards achieving robust reproducible nanosystems. As we considered the various approaches to address these threads and the various means by which collective effects can be harnessed, one that we did not discuss is the use of mechanical properties. The response of mechanical systems, limited in speed by velocity of sound, may still be able to provide a fast temporal response because of nanometer scale propagation distances. Nanotubes have been claimed to be mechanically robust and there are also examples of other materials that may perhaps have the necessary ductility. If true, it may be possible that the ability to mechanically deform and regain shape may provide an electromechanical switch that when implemented with a robust material provides a means to achieving low power characteristics. This is an area worth exploring to understand its properties, and if useful, the set of applications where the speeds are acceptable.

The critical question that future approaches have to address is related to minimizing the energy utilized in information processing while achieving the performance characteristics desired and dealing with the variability. Hierarchical approaches allow such apportionment of power dissipation and adaptive approaches help deal with variability. A suitable device that allows dynamic apportionment of power, while achieving desired performance characteristics, and with a suitable array of circuits and architectures is the challenge of nanoscale. One possibility is the use of self-aligned back-gated double-gate structures where threshold voltage can be dynamically tuned at speeds similar to that achievable by front gates. An example of such a device structure is shown in Fig. 3 [25, 26]. Circuits employing such a device can be made to work with changing supply voltages and changing threshold voltages so that minimum power is dissipated while achieving speed and noise margin characteristics desired. Fig. 3 also shows the tuning of power dissipation achievable by changing the threshold voltage in such an approach.

Figure 3: A cross-section of a self-aligned back-gated double gate transistor. The lower portion of the figure shows the tuning of power dissipation to achieve specific performance characteristics at 32 nm gate length..



VI. SUMMARY COMMENTS

Controlling nanoscale electronic phenomena, achieving appropriate device behavior – level of current, noise-margin, high yields, robust operation, hierarchy of design, and adaptation are critical to the success of a device in an application. Unique low temperature effects, mesoscopic device effects with resistances dominated by quantum conductances (q^2/h effects) which have impedances higher than of transmission lines, effects that do not provide adequate input-output isolation or gain, are all characteristics that while very interesting scientifically, are inappropriate for a practical large engineering system. Perhaps the most important characteristic for devices is the ability to achieve self averaging through multiple regions, an attribute that collective effects provide. This reduces statistical spread in device characteristics. Smallness, coherence, etc. defeat this. Locality is also critical. If circuit design becomes too dependent on events outside the region (defect tolerance e.g.) then circuit design is neither easy nor likely to give characteristics that are fruitful.

Acknowledgements

I am indebted to many of my students who have been instrumental in the practice of many of the ideas discussed here: Arvind Kumar, Chris Liu, Uygar Avci, Hao Lin, Helena Silva, Moon Kyung Kim. The work is supported by National Science Foundation through Center of Nanoscale Systems, Cornell Center of Materials Research, National Nanotechnology Infrastructure Network and Cornell Nanoscale Facility, Defense Advanced Research Project Agency, and Samsung/TND. Collaborations with colleagues at Cornell, Samsung and IBM are gratefully acknowledged.

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